MULTIMEDIA UNIVERSITY

STUDENT ID NO

MULTIMEDIA UNIVERSITY

FINAL EXAMINATION

TRIMESTER 1, 2015/2016

EEN4206 – SEMICONDUCTOR PACKAGING AND TEST

(ALL)

8 OCTOBER 2015
2.30 p.m - 4.30 p.m
(2 Hours)

INSTRUCTIONS TO STUDENTS

1. This Question paper consists of 3 pages with 5 Questions only.

2. Attempt **FOUR (4)** out of the **FIVE (5)** questions. All questions carry equal marks and the distribution of the marks for each question is given.

3. Please write all your answers in the Answer Booklet provided.

Question 1

(a)(i) What are the two main challenges in today's power packaging in System Application? [4 marks]

(ii) What are the potential components that can be integrated today in a complex system such as in a Double Clutch Transmission system? [3 marks]

(b)(i) Sketch the key package components of a power MOSFET and name the elements. [7 marks]

(ii) Write down five major electrical resistance components in the package construction. [6 marks]

(iii) Write down the Rth formula, name the components, and calculate the Max Capable Case Temperature for the following conditions:

Operating Temperature Range: –55 to 175 °C
Rth junction Ambient: 50K/W
Rth junction Case: 2K/W
Power Total at Case Level: 50W [5 marks]

Question 2

(a) Please name the five main keys of die attach process condition technology mainly adopted by semiconductor industries and its process technology. [5 × 2 marks]

(b) Briefly describe the process steps or process sequences for Solder Paste Die Attach process and each function of the process steps. [5 marks]

(c) Name the key compositions of Epoxy Mold Compound (EMC). [5 marks]

(d) Provide a description for the key compositions of Epoxy Mold Compound. [5 marks]

Continued .....

Question 3

(a) Explain the meaning of Nano technology. [2 marks]

(b) Explain how the photomask react with photoresist to form a pattern. Illustrate with a diagram for your explanation. [4 + 2 marks]

(c) Illustrate with a diagram of multilayer wafer cross section with transistor and indicate each layer with description. [4 marks]

(d) Illustrate with a diagram for the generic wafer process of wafer fabrication. [4 + 4 marks]

(e) What are the Process Control Monitoring (PCM) and Functional Wafer Test? [2 + 3 marks]

Question 4

(a) Explain the illumination modes in a normal high power scope and give the example of defect under each mode.
(i) Bright Field
(ii) Dark Field
(iii) Differential Interference Contrast (DIC) or Nomarki [3 × 2 marks]

(b) What are the common physical defects that can be detected using both x-ray microscopy and scanning acoustic microscopy? [3 marks]

(c) What are the purposes of annealing process in failure analysis? [4 marks]

(d)(i) What is de-capsulation process? [2 marks]

(ii) What are the chemicals used during de-capsulation process? [2 marks]

(e)(i) What is the conductive layer that commonly coated on the sample surface before any electron microscopy imaging? [2 marks]

(ii) What is the purpose of the conductive layer? [2 marks]

(f) List down four tools that can be used to investigate surface contamination. [4 marks]

Continued .....

Question 5

(a)(i) Define acceleration factor. [2 marks]

(ii) Calculate the acceleration factor by temperature cycling if the change in stress temperature = 125°C and the change in use temperature = 25°C, where power constant $C = 2$. [3 marks]

(iii) What are the lifetime requirements of products for the following applications?

Applications	Lifetime Requirement
Desktop computer	
Hand phone	
Automotive under the hood	
Telecom	
Trucks	

Based on the "time to failure under the use condition" given above, this product is suitable for which applications mentioned in the table above? [3 marks]

(b)(i) What is the key assumption in accelerated testing in terms of failure mode and/or mechanism? [2 marks]

(ii) Name the common acceleration variables applied during accelerated testing. [5 marks]

(iii) For the potential failure mechanisms listed below, what is the failure mode commonly detected?

Failure Mechanism	Failure Mode
Electrochemical corrosion	
Intermetallic compounds, Kirkendall voiding	
Mechanical stress between mould compound – wire	
Mechanical stress on chip	
Mobile ion contamination	
Contact spiking	

[6 marks]

(c) Describe how stress levels are chosen for accelerated testing? Explain how the stress loading is applied? [4 marks]

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